ABSTRACT OF THE DISCLOSURE

In a phase error detecting circuit used in a synchronous clock extracting circuit for extracting a clock which is synchronized with reproduced data, a cross reference value generator **72** inputs, as a rising cross reference value **S5**, rising phase error data **S3** calculated in a phase error calculator **71** to a rising cross detector **70a** and inputs, as a falling cross reference value **S6**, falling phase error data **S4** similarly calculated to a falling cross detector **70b**. Each of the cross detectors **70a** and **70b** calculates a difference value between the value of the reproduced data at a sampling point and the inputted cross reference value (cross offset value) **S5** or **S6** and outputs a rising or falling cross detection signal when one of two difference values at consecutive sampling points is negative and the other thereof is positive. Accordingly, a capture range is enlarged.